

FIG. 1

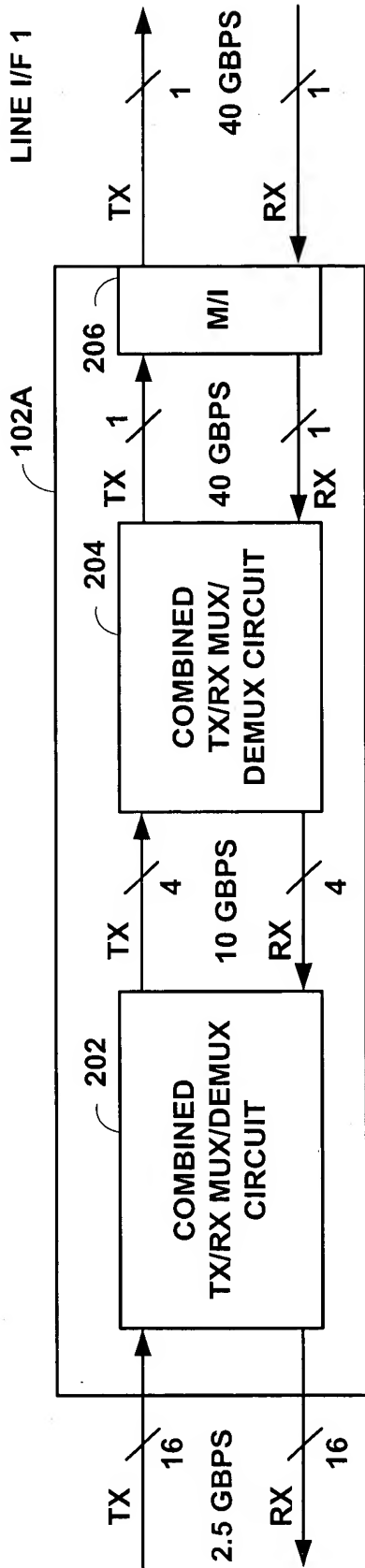


FIG. 2A

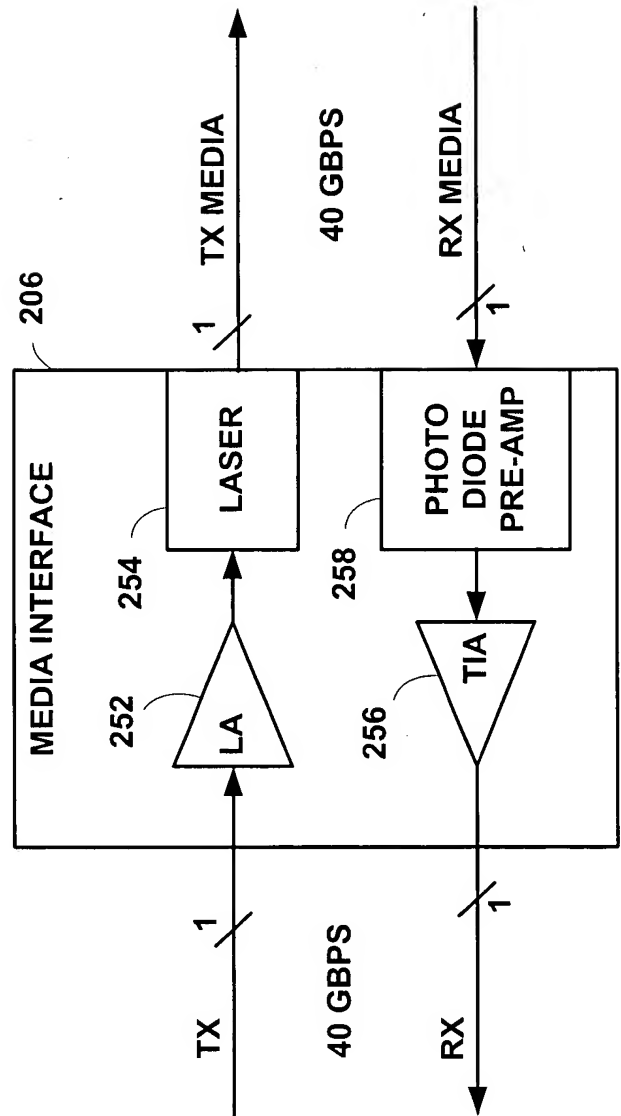


FIG. 2B

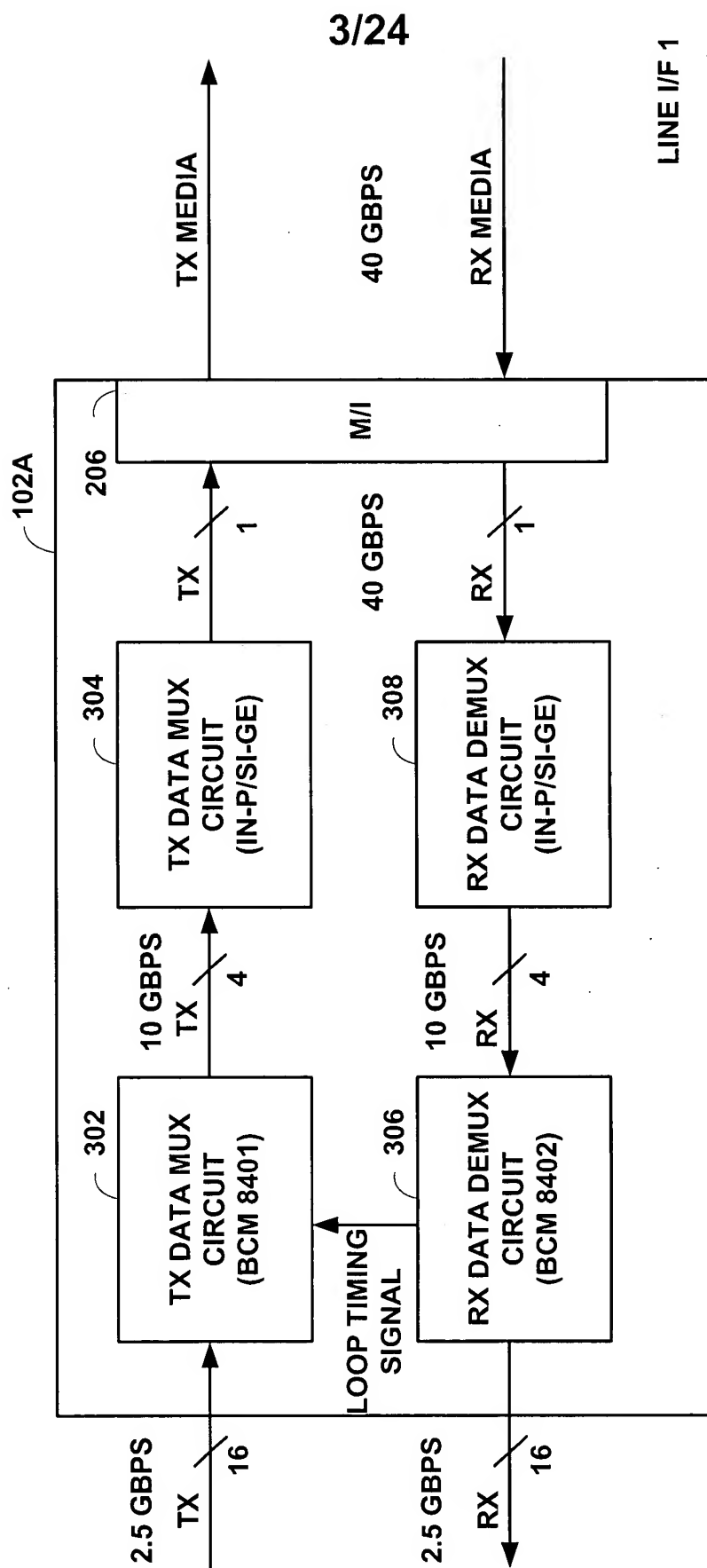


FIG. 3

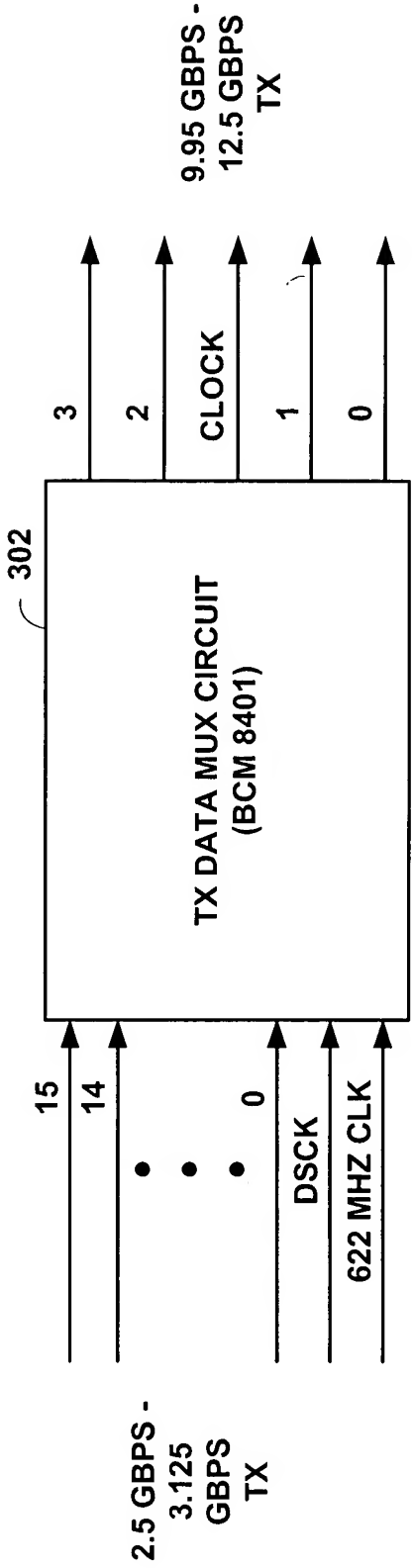


FIG. 4A

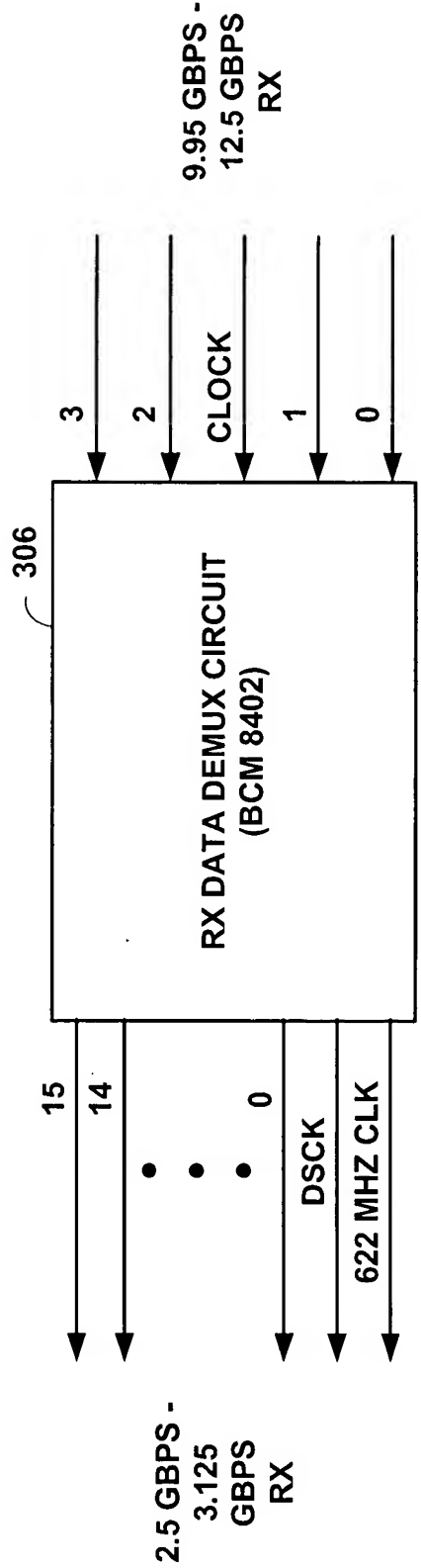


FIG. 4B

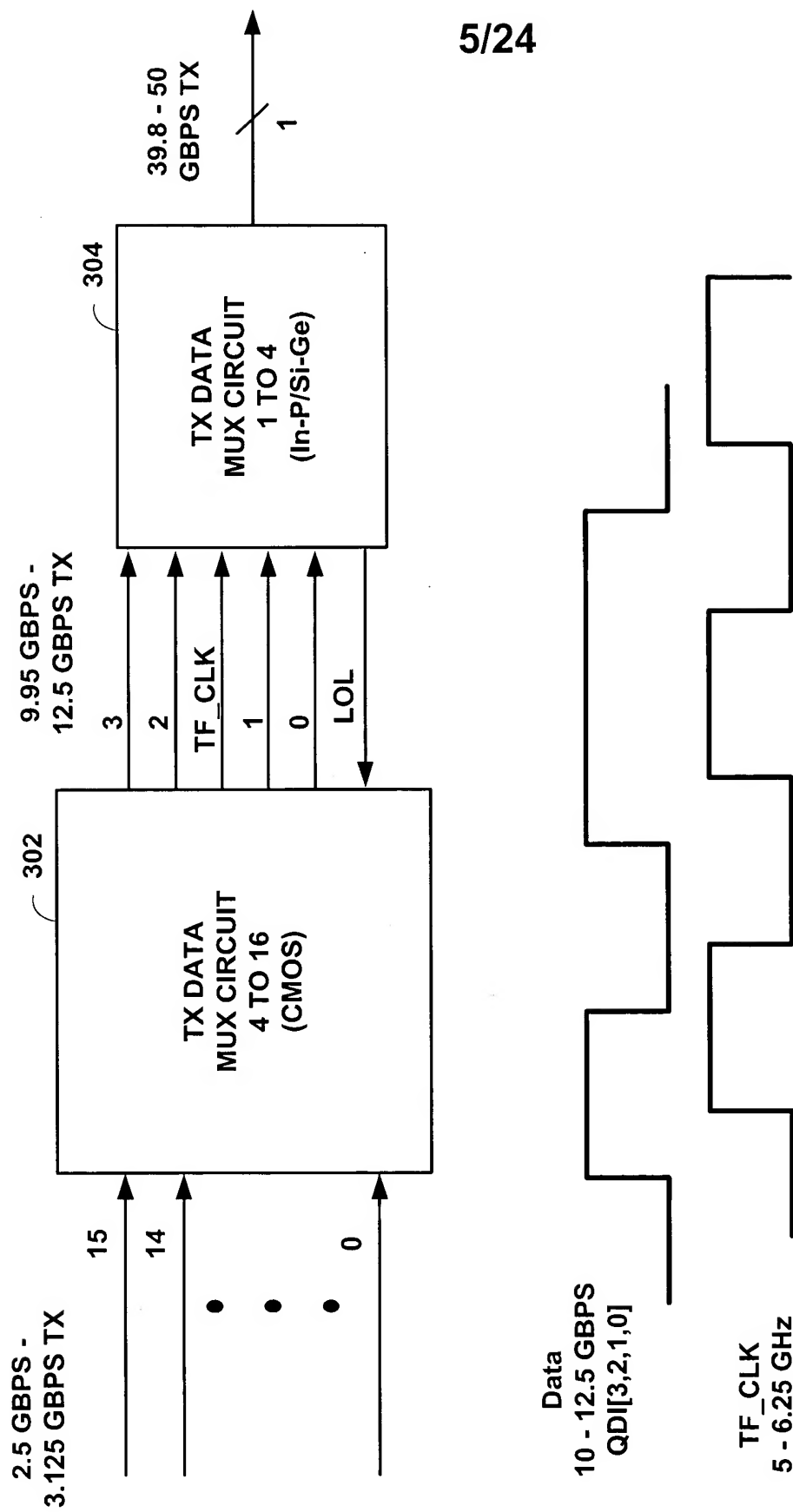


FIG. 5

Receiver Input and Source Centered Clock Performance

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output Common Mode	V _{cm}	See Figure Below	1575	1675	1775	mV
Single Ended Output Impedance	Z _{SE}		40	50	60	Ω
Differential Input impedance	Z _d		80	100	120	Ω
Input Impedance Mismatch	Z _M				10	%
Q40, CML Input Differential Amplitude, p-p	Δ VQDO	See Figure Below	400	500	600	mV
Q40 Input Rise and Fall Time (20% to 80%)	t _{RH} , t _{FH}			25	35	ps
Differential output return loss*	S11	Up to 7.5 GHz	10			dB
4-by-1 mux input return loss >15 db at 10 GHz						

400

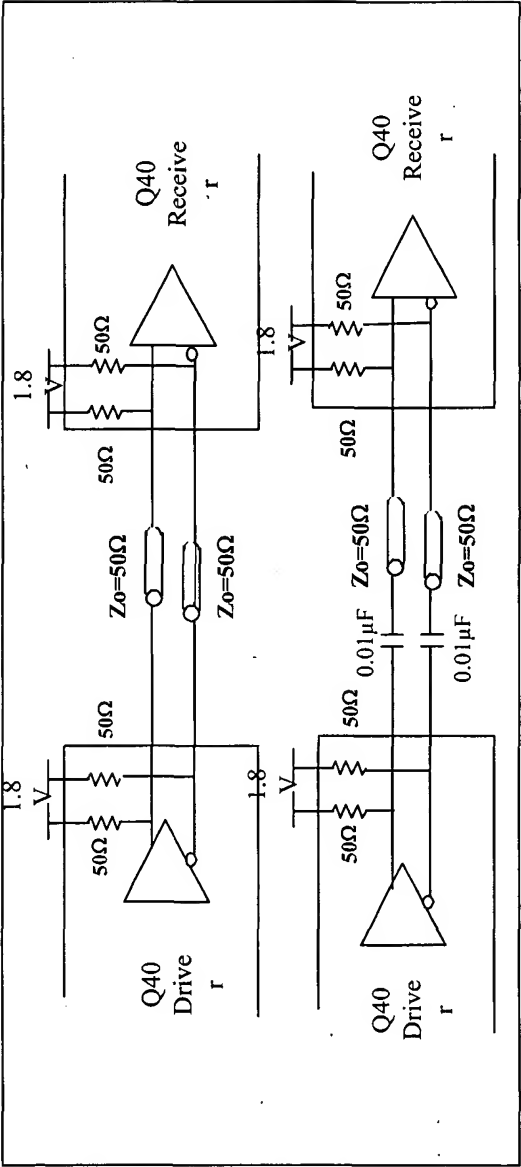


FIG. 6

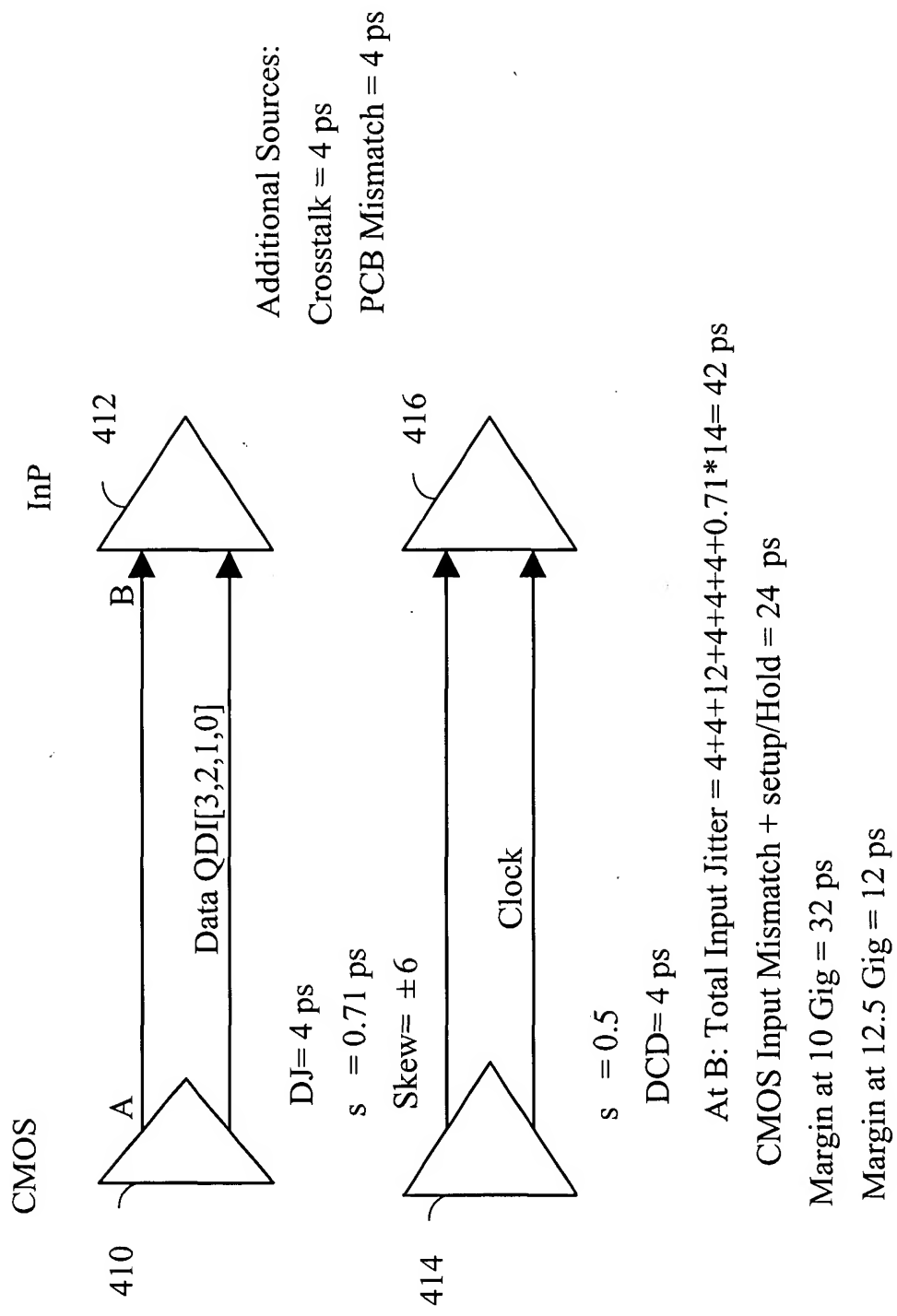


FIG. 7

Transmit and Receive

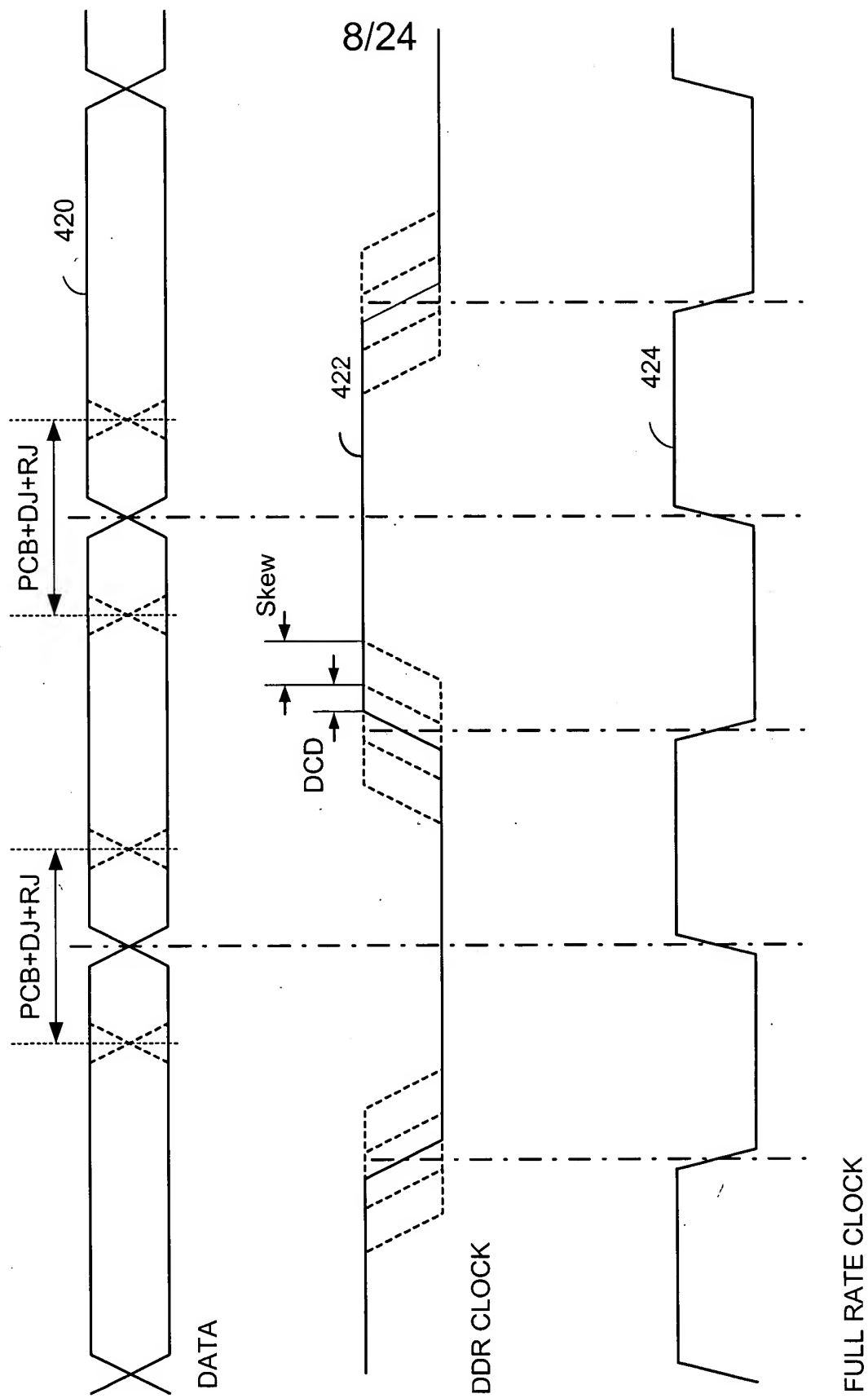


FIG. 8

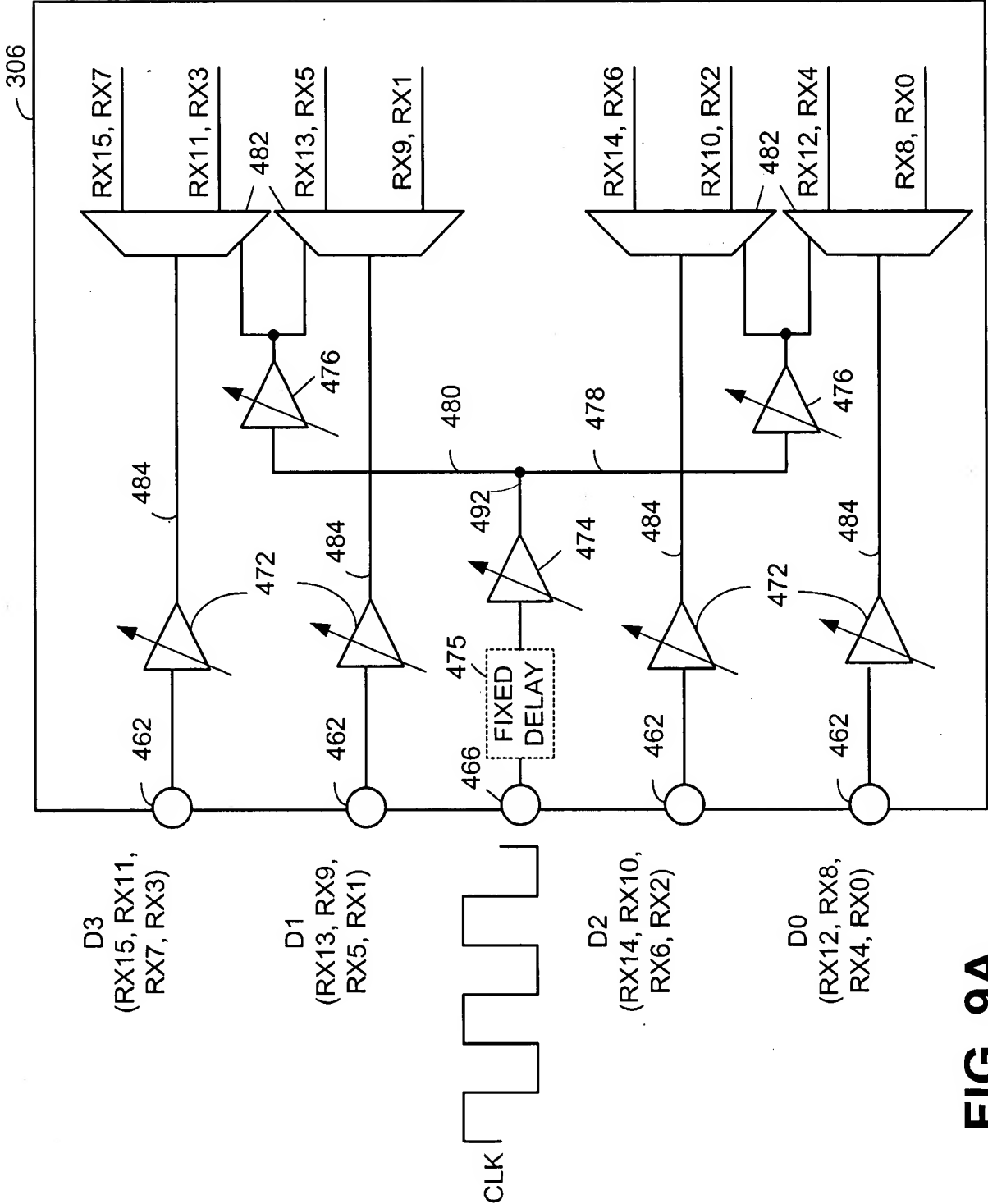


FIG. 9A



FIG. 9B

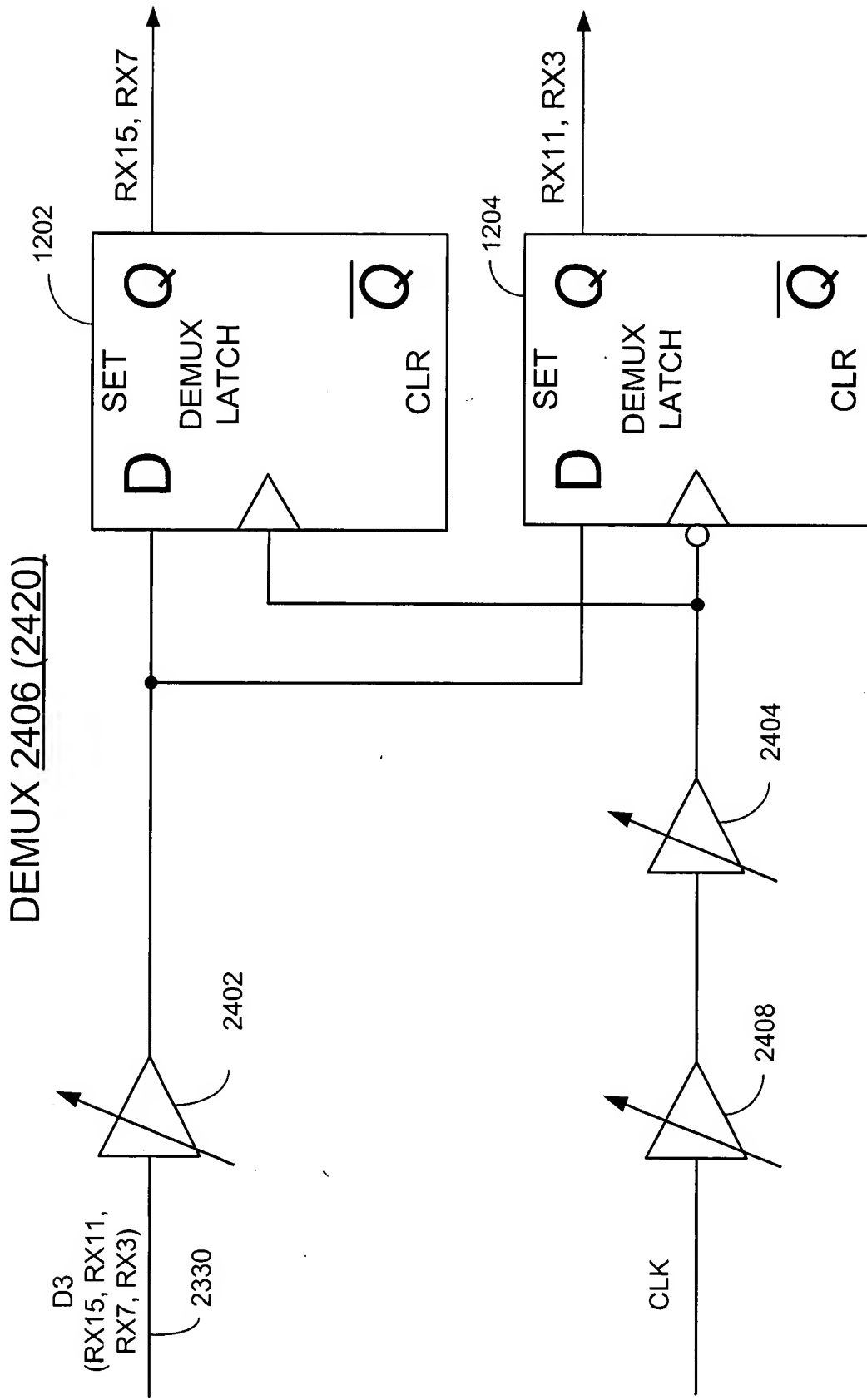


FIG. 10A

DEMUX LATCH 1202, 1204

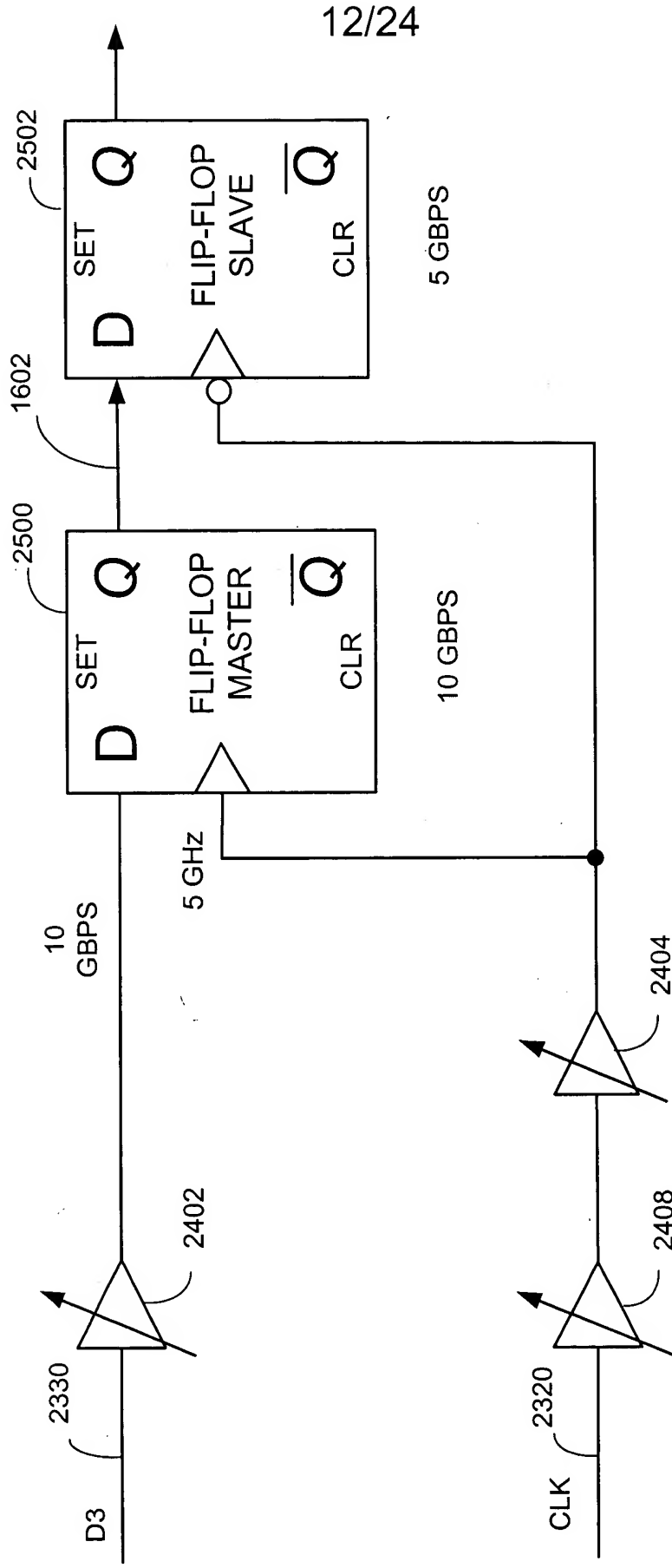


FIG. 10B

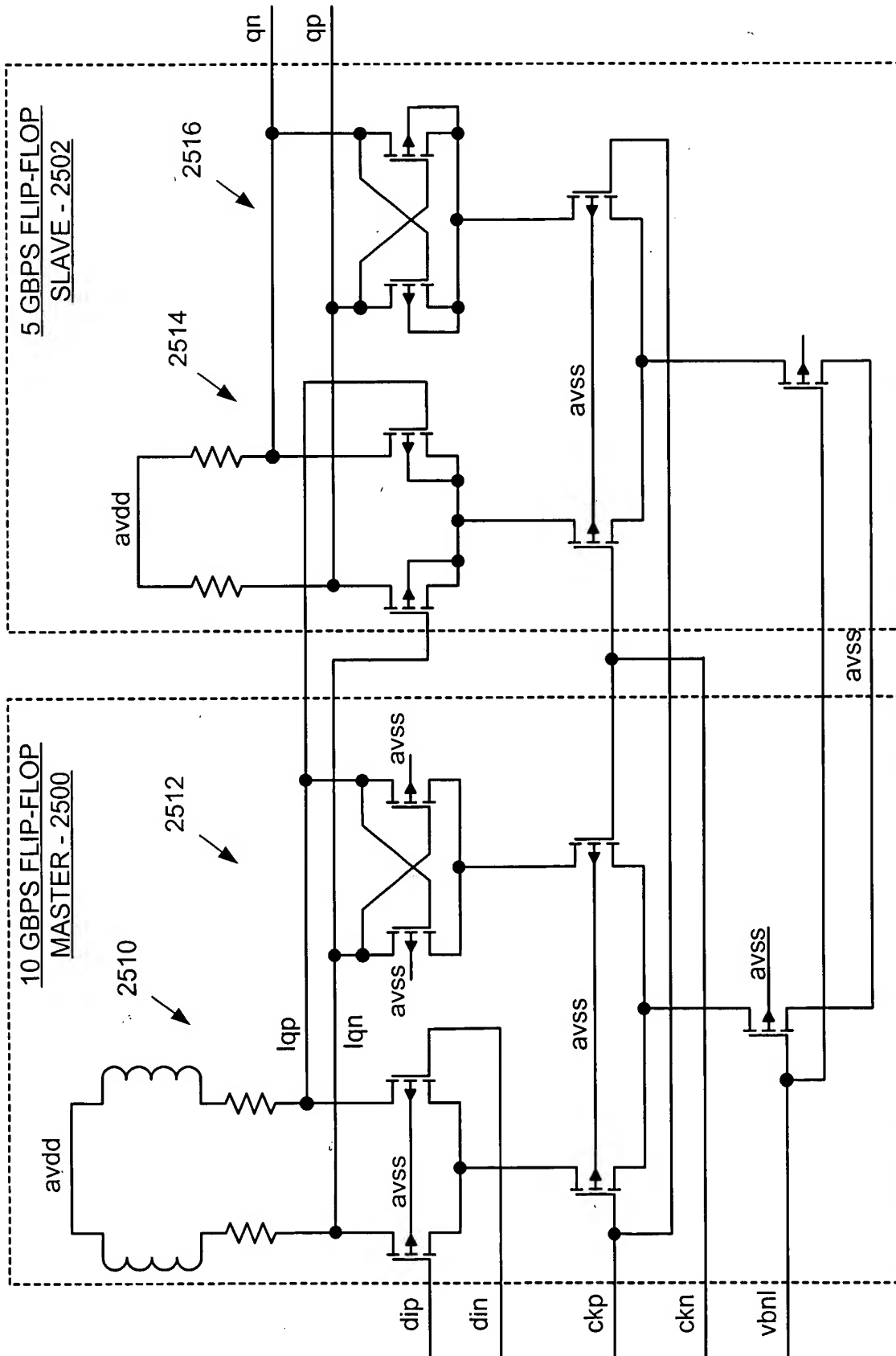


FIG. 10C

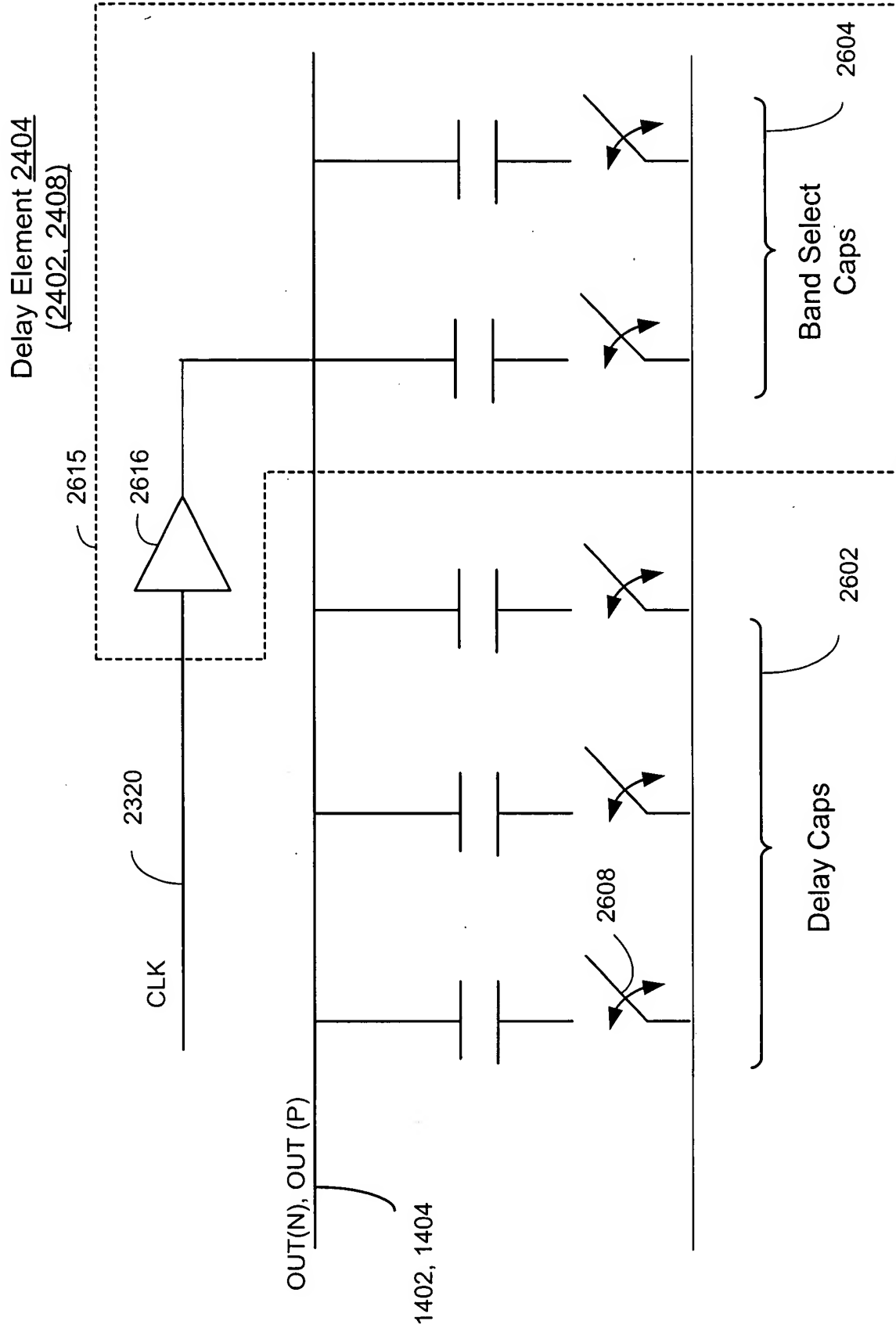


FIG. 11

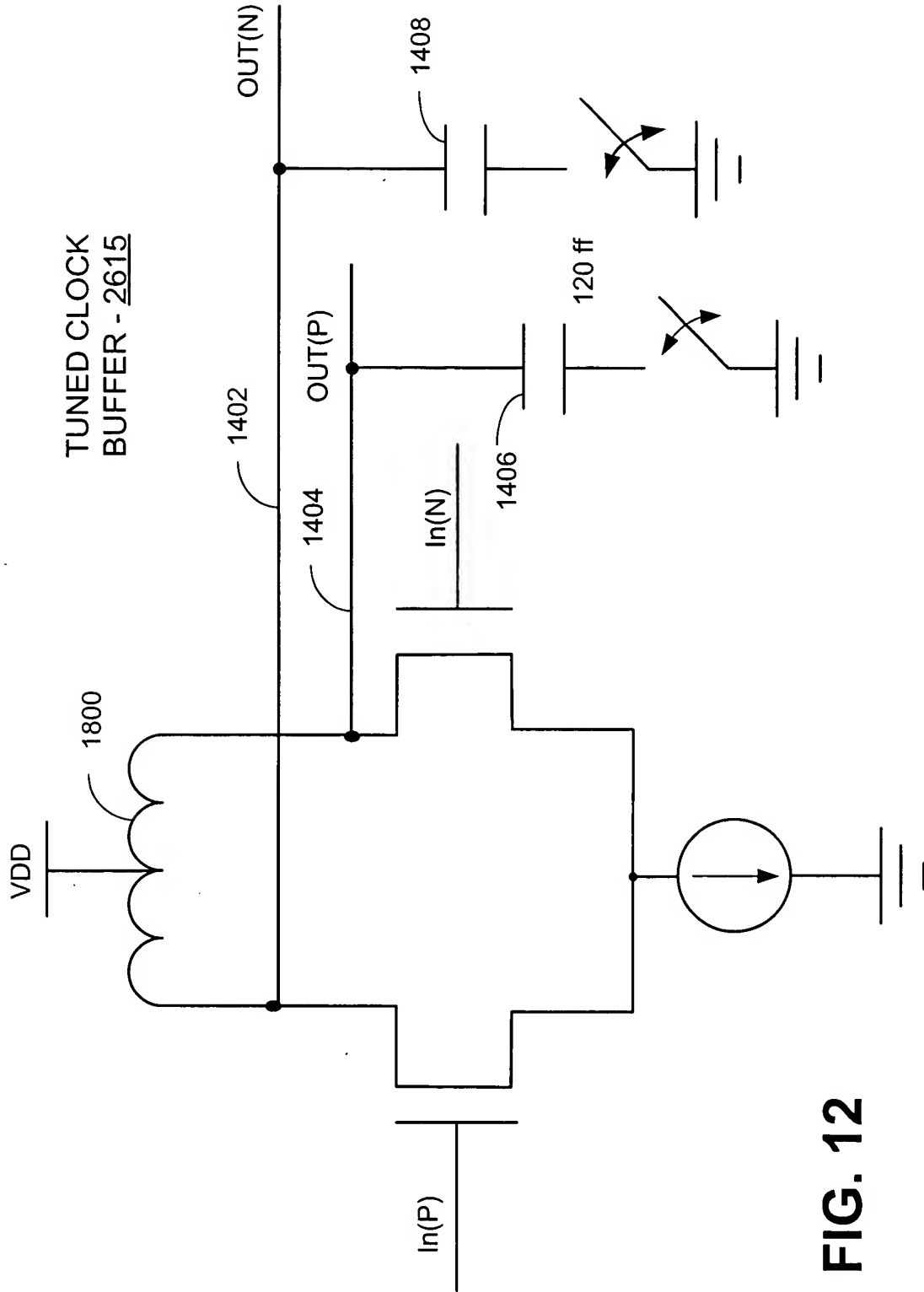


FIG. 12

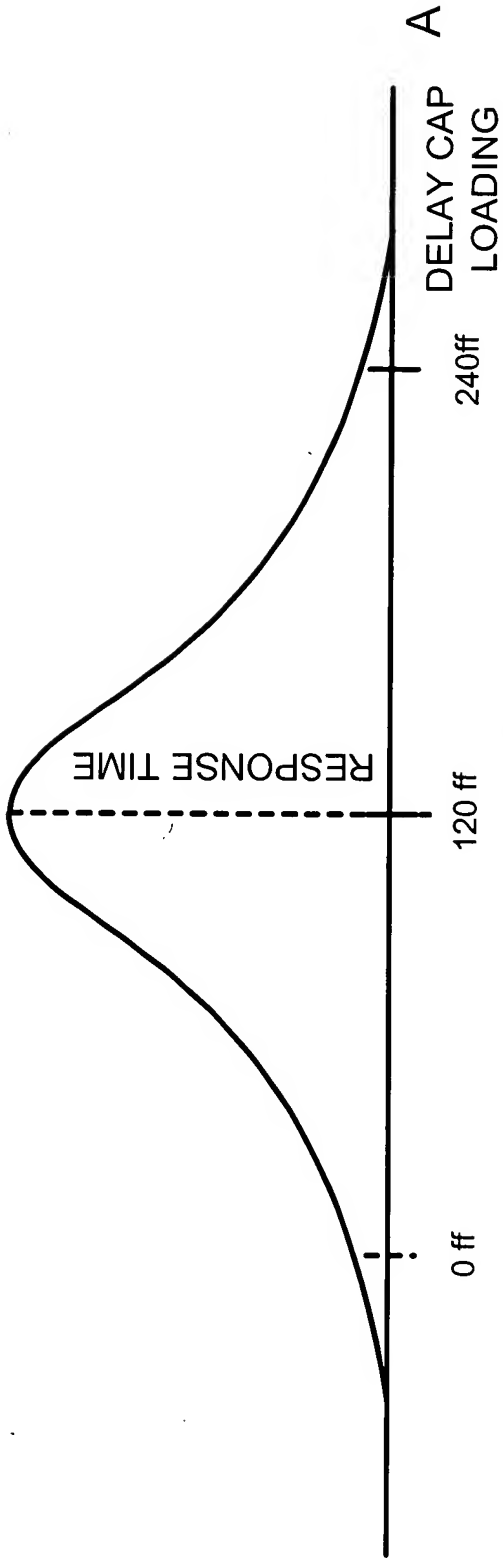


FIG. 13A

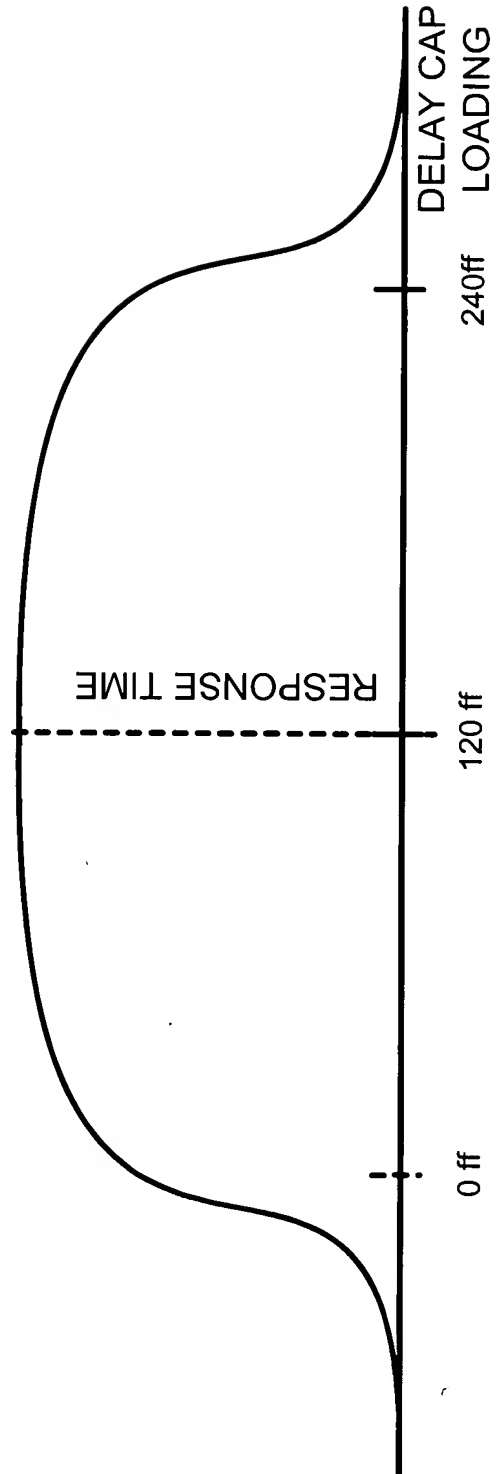


FIG. 13B

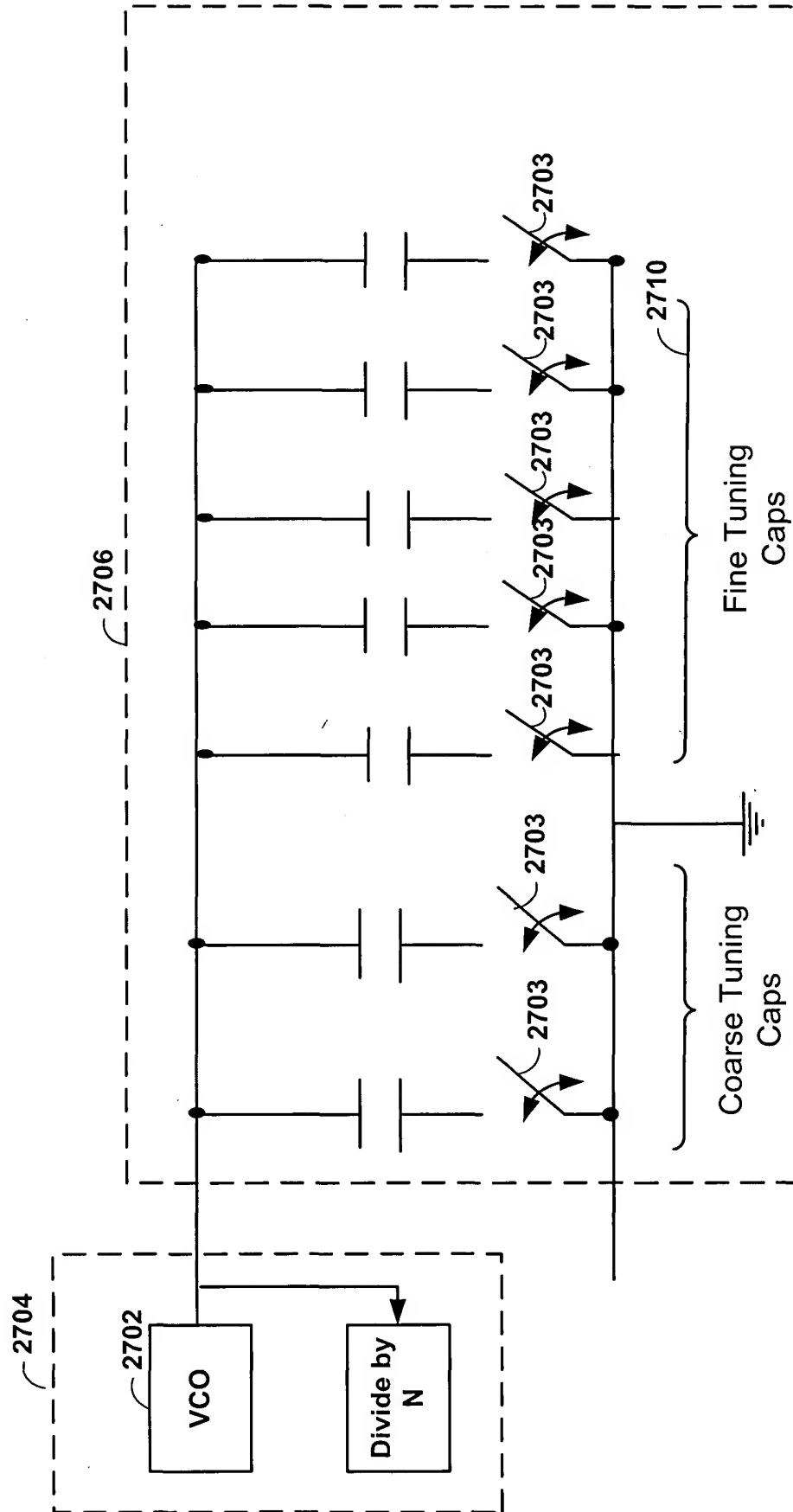


FIG. 14A

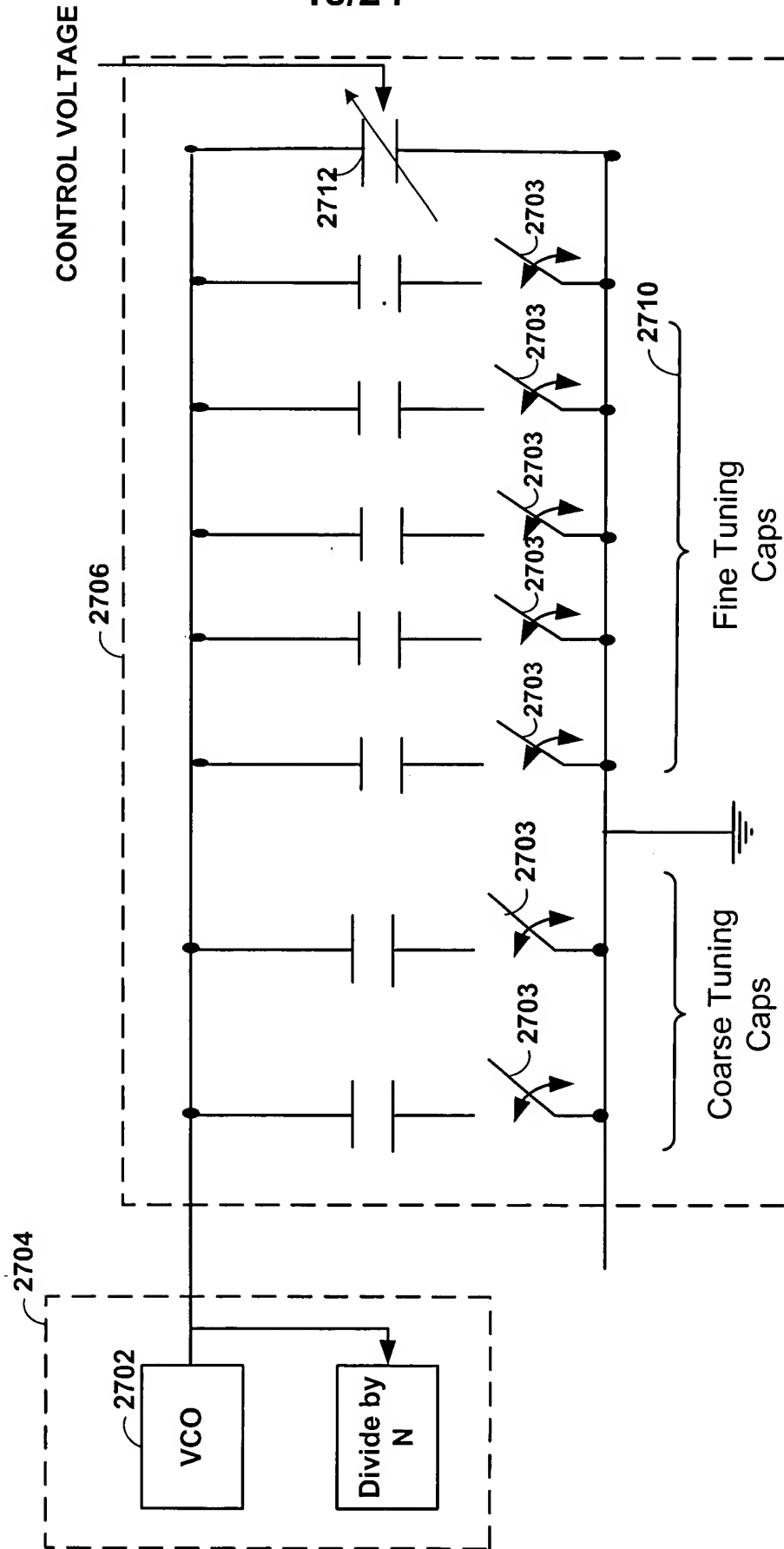


FIG. 14B

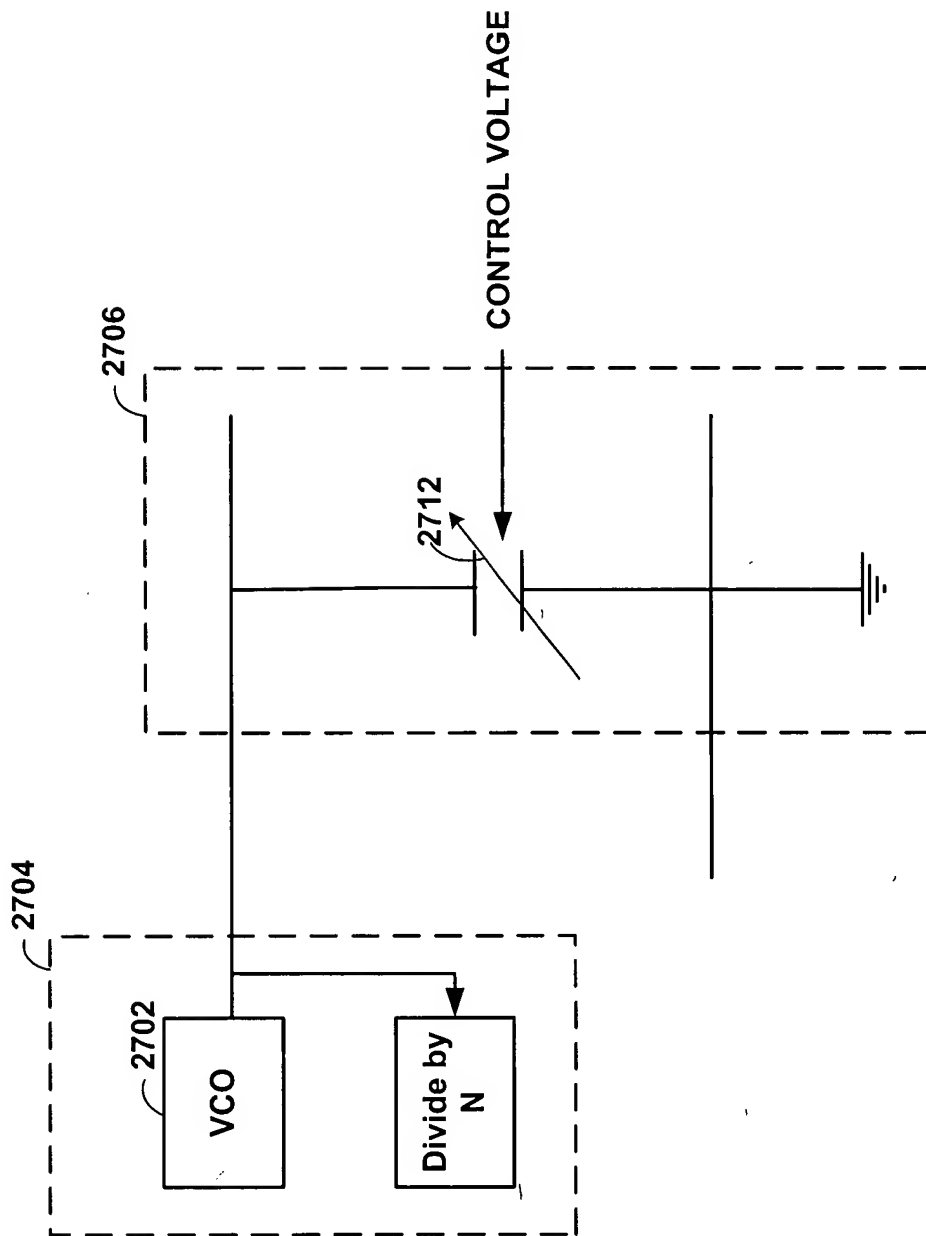


FIG. 14C

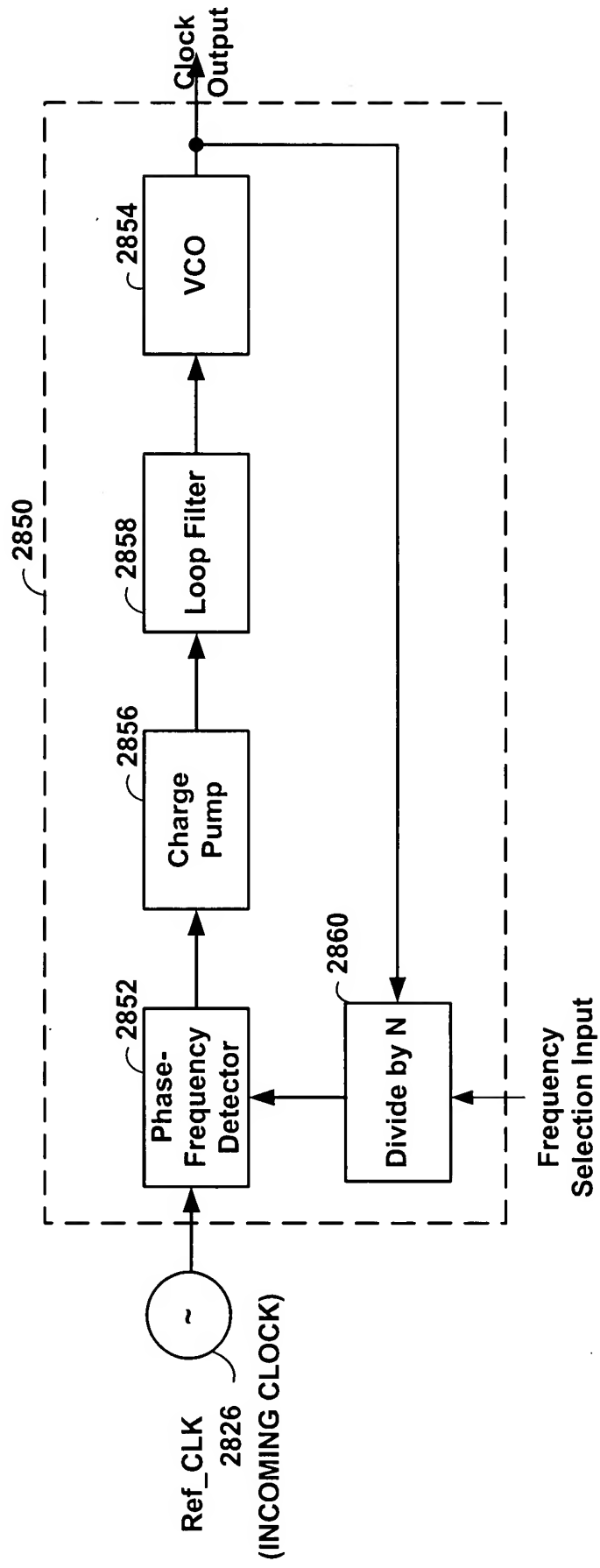


FIG. 15



FIG. 16A

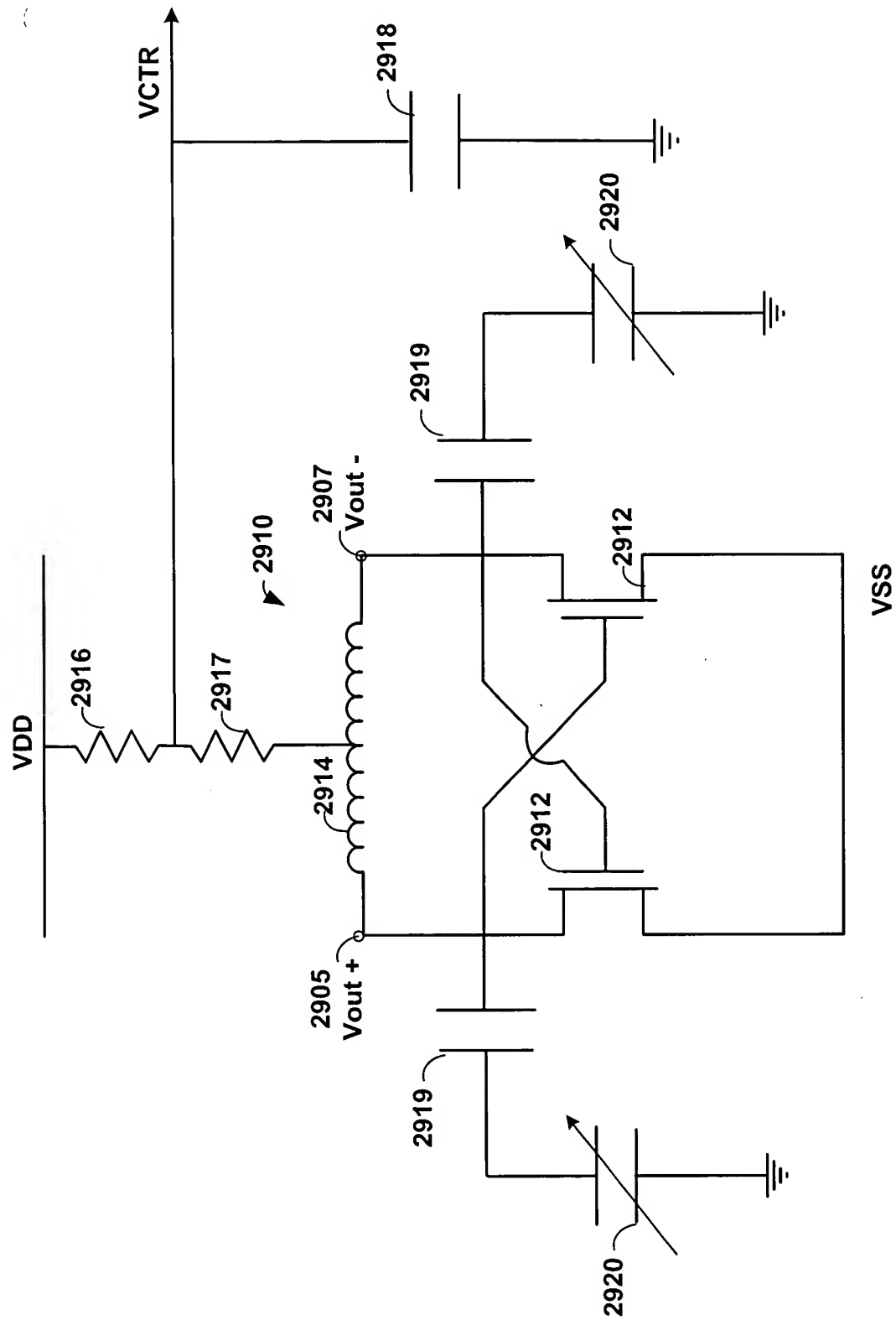


FIG. 16B

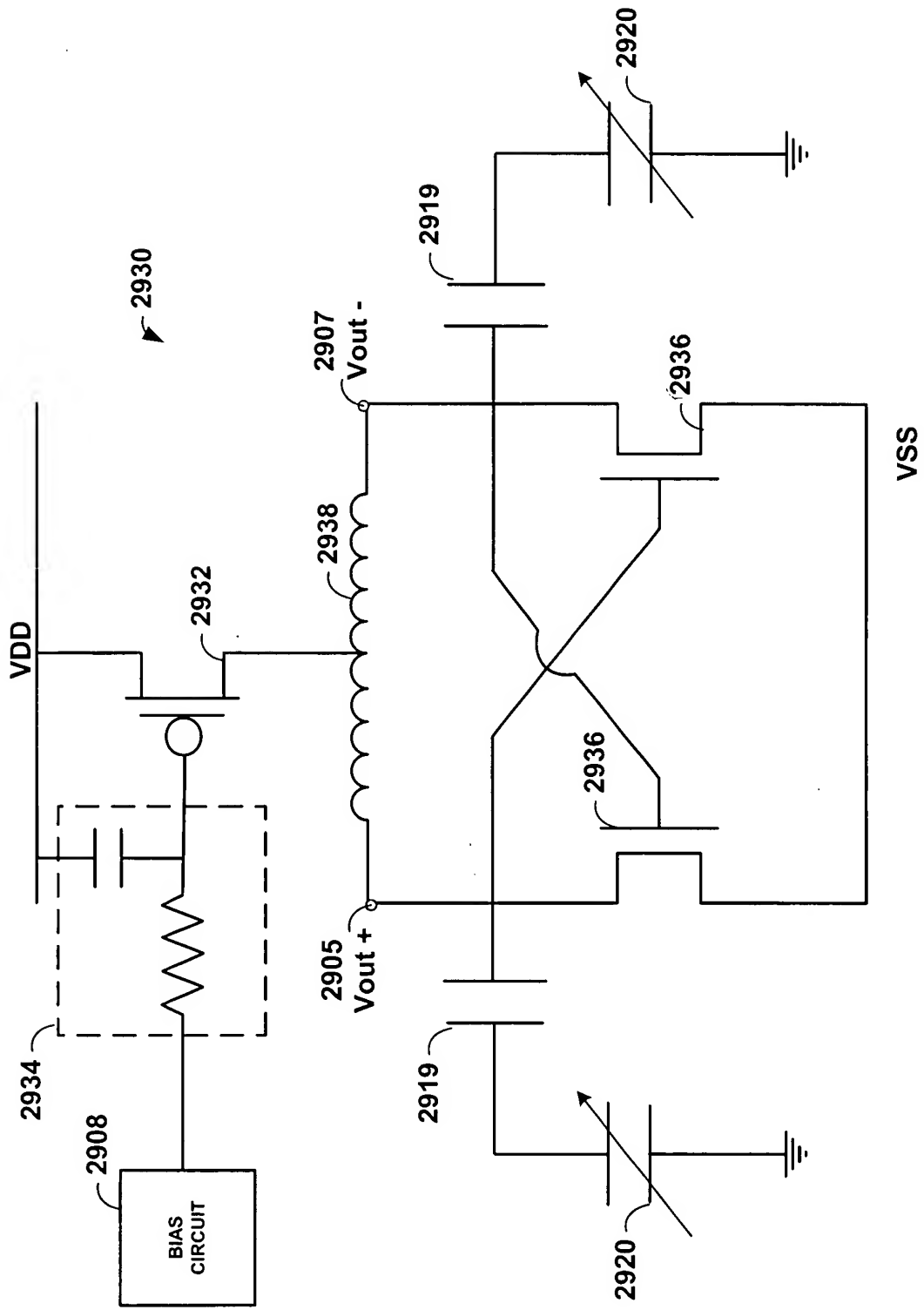


FIG. 16C

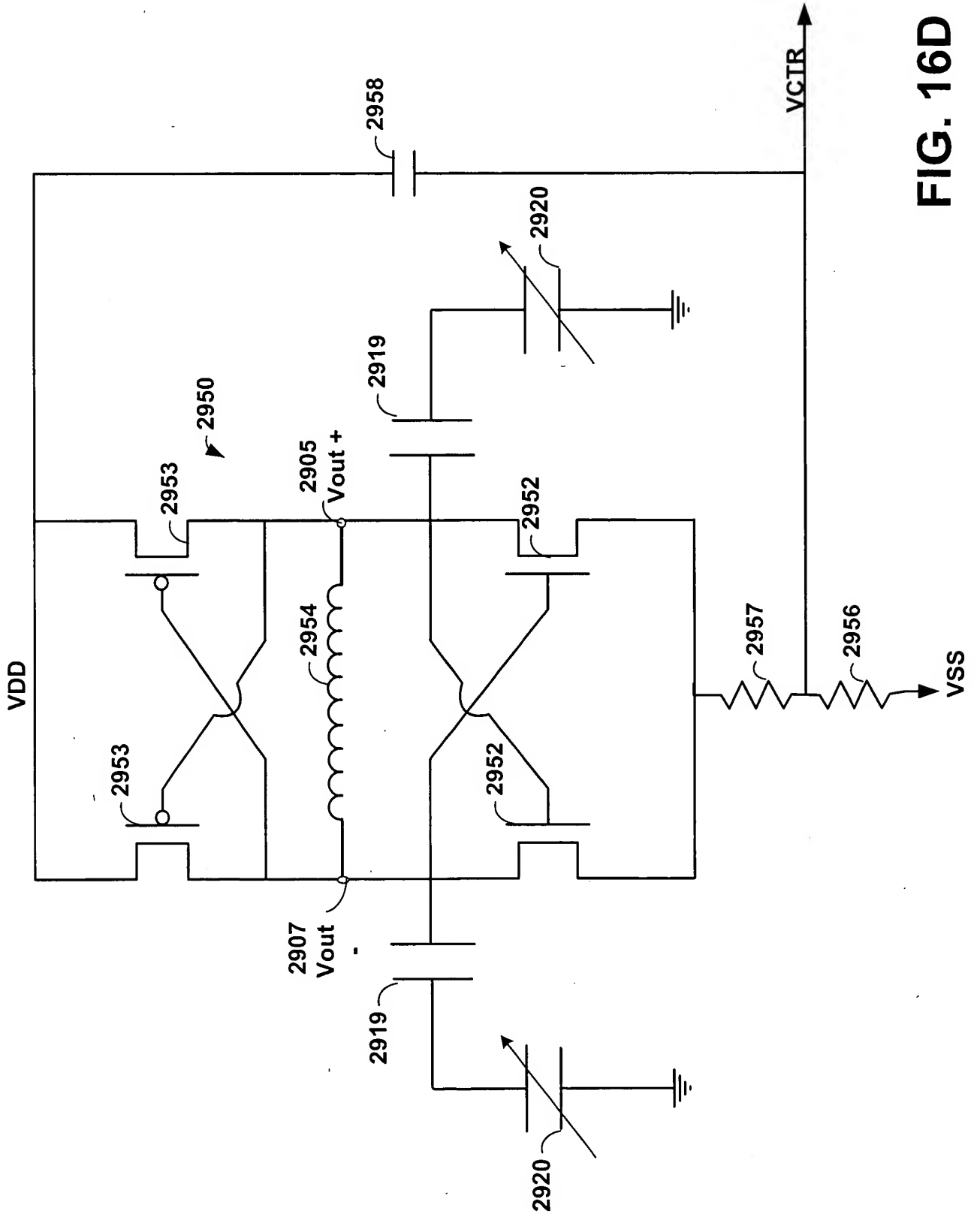


FIG. 16D